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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/822,021	03/30/2001	Ivo Koren	GR 98 P 8116 P	8447

7590 06/27/2005

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EXAMINER	
TRAN, NHAN T	

ART UNIT	PAPER NUMBER
2615	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,021	KOREN ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 3/7/2005 and are accepted. These drawings are Figures 1-4.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on applications filed in Germany on 09/30/1998 and PCT filed 09/17/1999. It is noted, however, that applicant has not filed certified copies of the 198 45 002.8 and PCT/DE99/02992 applications as required by 35 U.S.C. 119(b).

Response to Arguments

3. Applicant's arguments filed 3/7/2005 have been fully considered but they are not persuasive.

The Applicant argues that Tabei and Mangan do not teach a "double indexed" addressing procedure as required in claims 1 & 5 (Remarks, page 10). Specifically, the Applicant asserts that the bad bit pointers of Mangan do not include a pointer to a further memory, in which the actual address of the defect column is stored, and according to Mangan, the column number of the defective column is directly stored in the bad bit pointer (Remarks, page 13). The Applicant cites col. 8, lines 4-16 in Mangan and further asserts that the bad bit pointer in Mangan is, itself, is the column address.

In response, the Examiner respectfully disagrees with the Applicant. As cited by the Examiner in the previous Office Action, col. 8, lines 39-65 and Figs. 9A, 9B in Mangan clearly suggests "the bad column pointers can be included as part of each block, as are the bad bit pointers, but in this example are stored in a separate group of sectors duplicated within the memory array for this purpose." (col. 8, lines 53-56). It is clear that the bad bit pointer (pointer memory) is separate from bad column pointer (defect column memory) and that these pointers are set to point to each other in order for the bad bits and bad columns to be output properly. This is also seen from Fig. 9A, wherein a "double indexed" procedure is performed. It should be noted that a "double indexed" is not claimed. Accordingly, the claimed limitations are not necessarily considered as the Applicant's arguments for a "double indexed." Therefore, the combined teachings of Tabei and Mangan meet the claimed limitations of claims 1 & 5 for at least the reasons provided above and in the rejection section set forth below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tabei et al (US 5,805,216) in view of Mangan (US 5,471,478).

Regarding claim 5, Tabei discloses a device for correcting defective pixels of an image sensor, comprising:

an input receiving input pixel data (Fig. 5);

a defect memory unit (15) addressable with an image line number and an image column number, and having an output (see col. 3, line 60 – col. 4, line 3 and note that line number and column number is encompassed by "a position of a defective pixel");

an interpolator (14) connected to said input and receiving the input pixel data and having an output; a changeover switch connected to said interpolator and said controlled by a defect signal, said defect memory unit and changeover switch, in dependence on the defect signal, outputting either the input pixel data or output pixel data present at said output of said interpolator (see Fig. 5 & 6; col. 3, line 60 – col. 4, line 3 and col. 7, lines 56-65);

a comparator (16) connected to compare input image data (inherent column number) with the defective pixel position data from the defective memory and to form therefrom the defect signal (col. 3, line 60 – col. 4, line 3 and col. 7, lines 56-65).

Tabei does not explicitly teach the defect memory unit including a pointer memory, an address advancing device, and a defect column memory, whereby said pointer memory is addressed by the image line number and a content of address advancing device, said defect column memory, and said cell thus addressed addresses, via said address advancing device, said defect column memory, and said defect column memory outputs a defect column number for the line with the relevant image line number.

Mangan teaches reading out data stored in a semiconductor memory (e.g., EEPROM) that includes a pointer memory, an address advancing device (for incrementing column/row), and a

defect column memory whereby the pointer memory is addressed by row number and a content of a cell thus addressed addresses defect column memory via address advancing device. The defect column memory outputs a defect column number for the row with the relevant image line number (see Figs. 3, 4, 9A & 9B; col. 8, lines 39-65).

Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Mangan with Tabei for reading out of the defective pixel locations from the defective memory by using line and column pointers as taught by Mangan to arrive at the Applicant's claimed invention so that accessing to the defective pixel positions is performed in a short time since the defective pixel positions have been pointed by loading row and column pointers in a memory map/table prior to taking image in.

Regarding claim 6, Mangan further discloses that the defect column memory is configured with one continuation bit (i.e., a single pointer) per defect column number (col. 8, lines 48-53), and wherein the address advancing unit is controllable by the continuation bit (Figs. 9A & B and col. 8, lines 57-65).

Regarding claim 7, also disclosed by Mangan is that comparator connected to ascertain whether the defect column number is smaller than the column number (step 371, Fig. 9A), and wherein the address advancing device advances the address of the defect column memory if the continuation bit is set (see Fig. 9A and col. 8, lines 56-65).

Regarding claim 1, the method claim 1 is encompassed by the analysis of claim 5.

Regarding claim 2, Mangan further discloses storing pointer in the pointer memory and the column numbers in the defect column memory in such a way that in a first case with multiple defect pixels in the columns of a line (Fig. 8B, col. 8, lines 16-20), the pointer belonging to the line addresses a memory cell in the defect column memory that contains a first of the column numbers, and the column numbers of the further defective columns increasing order (by incrementing) in subsequent memory cells of the defect are deposited column memory (col. 8, lines 56-65);

in a second case with multiple defective pixels in a column, the pointers of multiple different lines refer to the same cell of the defect column memory with the associated defect column number (Fig. 8A & B; col. 5, lines 19-30 and note steps 341, 343, 345, 349, 351 wherein the multiple defective cells in a common column are pointed).

in a third case without defective pixels in a line, a cell in the defect column memory provided specifically for this case is addressed with the associated pointer (see steps 347, 355 in Fig. 8B and col. 8, lines 10-14 or steps 375, 381 in Fig. 9A for indication of no defective cells in a row).

Regarding claim 3, inherent in the combination of Tabei and Mangan is that during reading of a subimage (i.e., 3x3 subimage), overreading and not correcting defect column numbers which are smaller than the column numbers of the subimage. Since any defect column numbers that are **outside** of a normal subimage (in a case no defective pixels in this 3x3

subimage), there is no correction for such the outside defect column numbers (encompasses smaller column numbers) during reading out of the normal 3x3 subimage.

Regarding claim 4, see the analysis of claim 6, wherein a last respective defect column of a respective line is identified when "NO" is recognized in step 371, Fig. 9A.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 8:00am - 6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

DAVID L. OMETZ
PRIMARY EXAMINER